What is claimed is:

1. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a dielectric layer pattern having an ONO composition on a substrate;

forming a polysilicon layer on the substrate including over the dielectric layer pattern;

patterning the polysilicon layer to form a polysilicon layer pattern on the dielectric layer pattern, wherein the polysilicon layer pattern has a split structure that exposes a portion of the dielectric layer pattern;

etching the exposed portion of the dielectric layer pattern; and

subsequently implanting impurities into the substrate to form source/drain regions in the substrate.

2. The method of claim 1, wherein said forming of the dielectric layer pattern comprises:

forming a first oxide film having a thickness of about 20 to about 100 Å on the substrate,

forming a nitride film having a thickness of about 20 to about 100 Å on the first oxide film,

forming a second oxide film having a thickness of about 20 to about 100 Å on the nitride film,

forming an etching mask on the second oxide film, and

etching the second oxide film, the nitride film and the first oxide film using the etching mask.

3. The method of claim 1, and further comprising forming a gate oxide film on the substrate by oxidizing a surface of the substrate after the dielectric layer pattern is formed.

4. The method of claim 1, further comprising oxidizing a surface of the polysilicon layer pattern.

5. The method of claim 1, wherein said etching of the exposed portion of the dielectric layer pattern comprises removing only some of the entire thickness of the exposed portion of the dielectric layer pattern, wherein a remainder of the portion of the dielectric layer pattern, exposed by the split polysilicon layer pattern, is left on the substrate.

6. The method of claim 1, wherein said implanting of ions comprises a first implantation process using the polysilicon layer pattern as a mask to form a source region in the substrate having a vertical profile and a width substantially identical to the width of the exposed portion of the dielectric layer

7. The method of claim 1, wherein said implanting of ions comprises:

forming preliminary source/drain regions at portions of the substrate exposed by the polysilicon layer pattern,

subsequently forming a nitride layer on the substrate including over the polysilicon layer pattern,

etching back the nitride layer to form a spacer on a sidewall of the polysilicon layer pattern, and

subsequently forming lightly doped drain (LDD) structures using the polysilicon layer pattern and the spacer as a mask.

8. The method of claim 7, wherein said forming of the preliminary source/drain regions is performed by implanting impurities of Group V with a relatively low ion implantation energy of about 3 to about 15 KeV, and said forming of the lightly doped drain (LDD) structures is performed by implanting impurities of Group V with a relatively high ion implantation energy of about 20 to about 50 KeV.

9. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a dielectric layer pattern having an ONO composition on a substrate;

oxidizing portions of the substrate exposed by the dielectric layer pattern;

subsequently forming a polysilicon layer on the substrate including over the dielectric layer pattern;

patterning the polysilicon layer to form a polysilicon layer pattern on the dielectric layer pattern, wherein the polysilicon layer pattern has a split structure that exposes a portion of the dielectric layer pattern;

etching the exposed portion of the dielectric layer pattern;

subsequently implanting ions into the substrate to form preliminary source/drain regions in the substrate;

subsequently forming a spacer on a sidewall of the polysilicon layer pattern; and

subsequently implanting ions into the substrate using the polysilicon layer pattern and the spacer as a mask to form lightly doped drain (LDD) structures.

10. The method of claim 9, wherein said forming the dielectric layer pattern comprises:

forming a first oxide film having a thickness of about 20 to about 100 Å on the substrate,

forming a nitride film having a thickness of about 20 to about 100 Å on the first oxide film,

forming a second oxide film having a thickness of about 20 to about 100 Å on the nitride film,

forming an etching mask on the second oxide film, and

etching the second oxide film, the nitride film and the first oxide film using the etching mask.

11. The method of claim 9, further comprising oxidizing a surface of the polysilicon layer pattern.

12. The method of claim 9, wherein said etching of the exposed

portion of the dielectric layer pattern comprises removing only some of the entire thickness of the exposed portion of the dielectric layer pattern, wherein a remainder of the portion of the dielectric layer pattern, exposed by the split polysilicon layer pattern, is left on the substrate.

13. The method of claim 9, wherein said forming of the spacer comprises:

forming a nitride layer on the substrate including over the polysilicon layer pattern, and

etching back the nitride layer.

14. The method of claim 9, wherein said forming of the preliminary source/drain regions is performed by implanting impurities of Group V with a relatively low ion implantation energy of about 3 to about 15 KeV, and said forming of the lightly doped drain (LDD) structures is performed by implanting impurities of Group V with a relatively high ion implantation energy of about 20 to about 50 KeV.

15. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a dielectric layer pattern on a substrate;

forming a gate layer on the substrate including over the dielectric layer pattern;

patterning the gate layer to form a gate layer pattern on the dielectric layer

pattern, wherein the gate layer pattern has a split structure that exposes a portion of the dielectric layer pattern;

removing only some of the entire thickness of the exposed portion of the dielectric layer pattern, wherein a remainder of the portion of the dielectric layer pattern, exposed by the split gate layer pattern, is left on the substrate;

subsequently implanting impurities into the substrate using the split gate layer pattern as a mask to form a source region in the substrate.

16. The method of claim 15, wherein said implanting of impurities removes said remainder of the portion of the dielectric layer pattern.

17. The method of claim 15, further comprising:

subsequently forming a nitride layer on the substrate including over the split gate layer pattern,

etching back the nitride layer to form a spacer on a sidewall of the gate layer pattern, and

implanting ions into the substrate using the gate layer pattern and the spacer as a mask.

18. The method of claim 16, further comprising:

subsequently forming a nitride layer on the substrate including over the gate layer pattern,

etching back the nitride layer to form a spacer on a sidewall of the gate layer pattern, and

implanting ions into the substrate using the gate layer pattern and the spacer as a mask.

19. The method of claim 15, wherein said forming of the dielectric layer pattern comprises forming a first oxide or oxynitride layer, a nitride layer, and a second oxide layer one atop the other.

20. The method of claim 19, wherein said removing only some of the entire thickness of the exposed portion of the dielectric layer pattern comprises removing only said second oxide layer and said nitride layer, wherein the remainder of the dielectric pattern on the substrate serves as a buffer layer during the implanting of ions to form the source region.